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(71) Applicants
Kabushiki Kaisha Toshiba

(Incorporated in Japan)

72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken, Japan

(72) Inventor
Hideyuki Hagino

(74) Agent and/or Address for Service
Haseltine, Lake & Co, Hazlitt House, 28 Southampton Buildings, Chancery Lane, London WC2A 1AT

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H4F H3G
Selected US specifications from IPC sub-classes H04N H03G

# (54) Automatic gain control circuit

(57) An automatic gain control (AGC) circuit for performing AGC on a picture signal includes an amplifier 1 for amplifying the picture signal, a clamping circuit 2 for fixing a tip-end level of a synchronous signal component of the picture signal to a given level, a synchronous detection AGC loop formed by the amplifier 1, the claming circuit 2, a synchronous detection circuit 3 and a first filter 5, a peak detection AGC loop formed by the amplifier 1, a peak detection circuit 4 and a second filter 6, and a precharging means 9 connected between the first filter 5 and the second filter 6 for charging the second filter 6 by a voltage which follows a voltage charge on the first filter 5 when the synchronous detection AGC loop is activated but the peak detection AGC loop is deactivated.

FIG. 2.

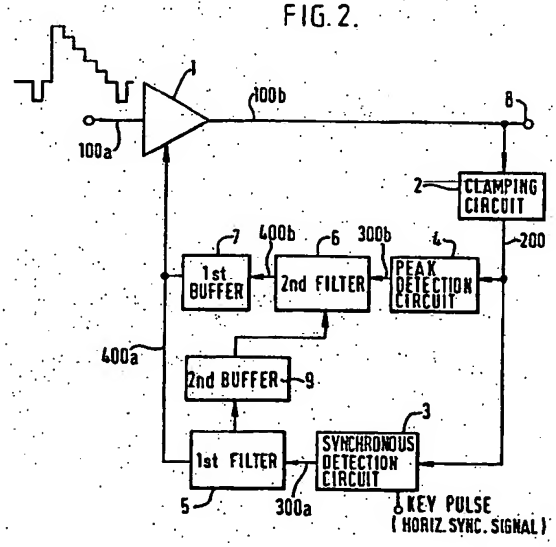


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FIG. 1.
PRIOR ART

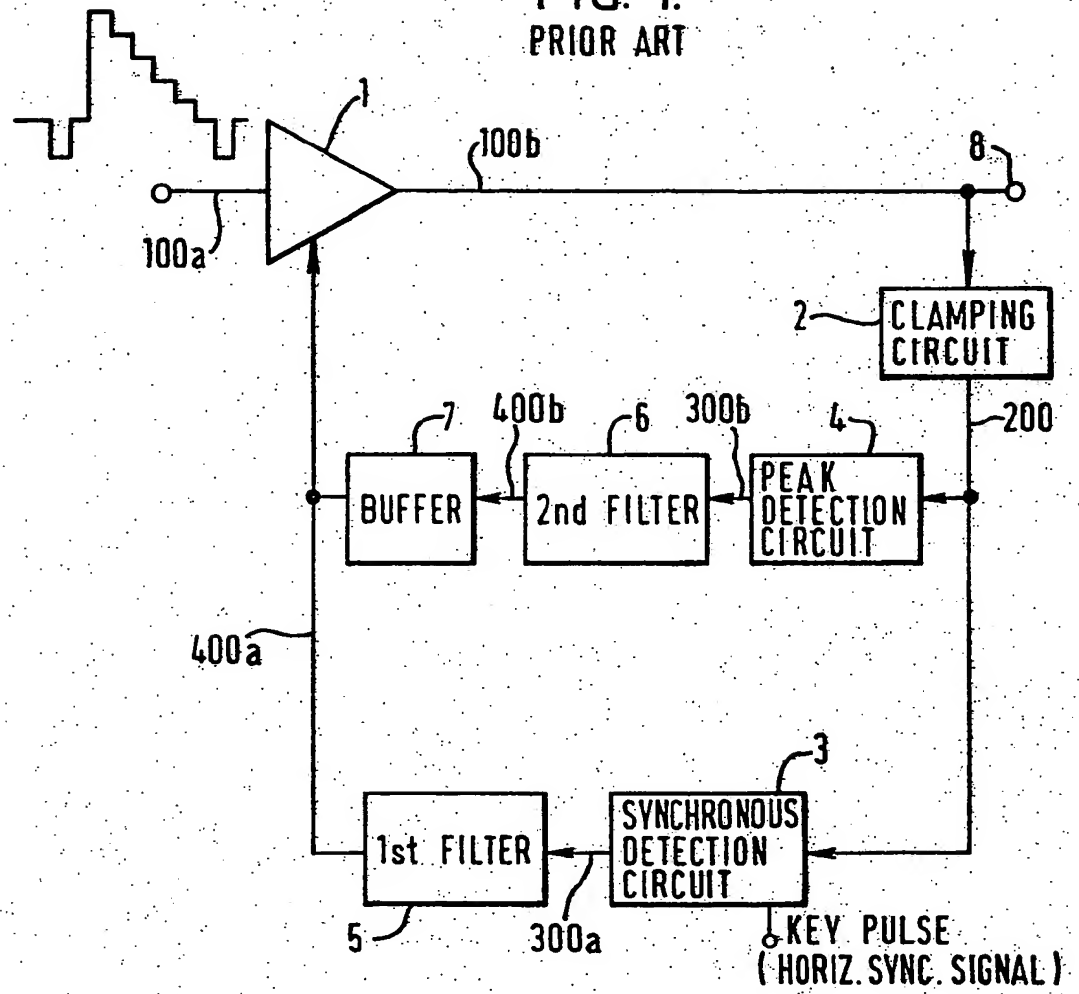


FIG. 2.

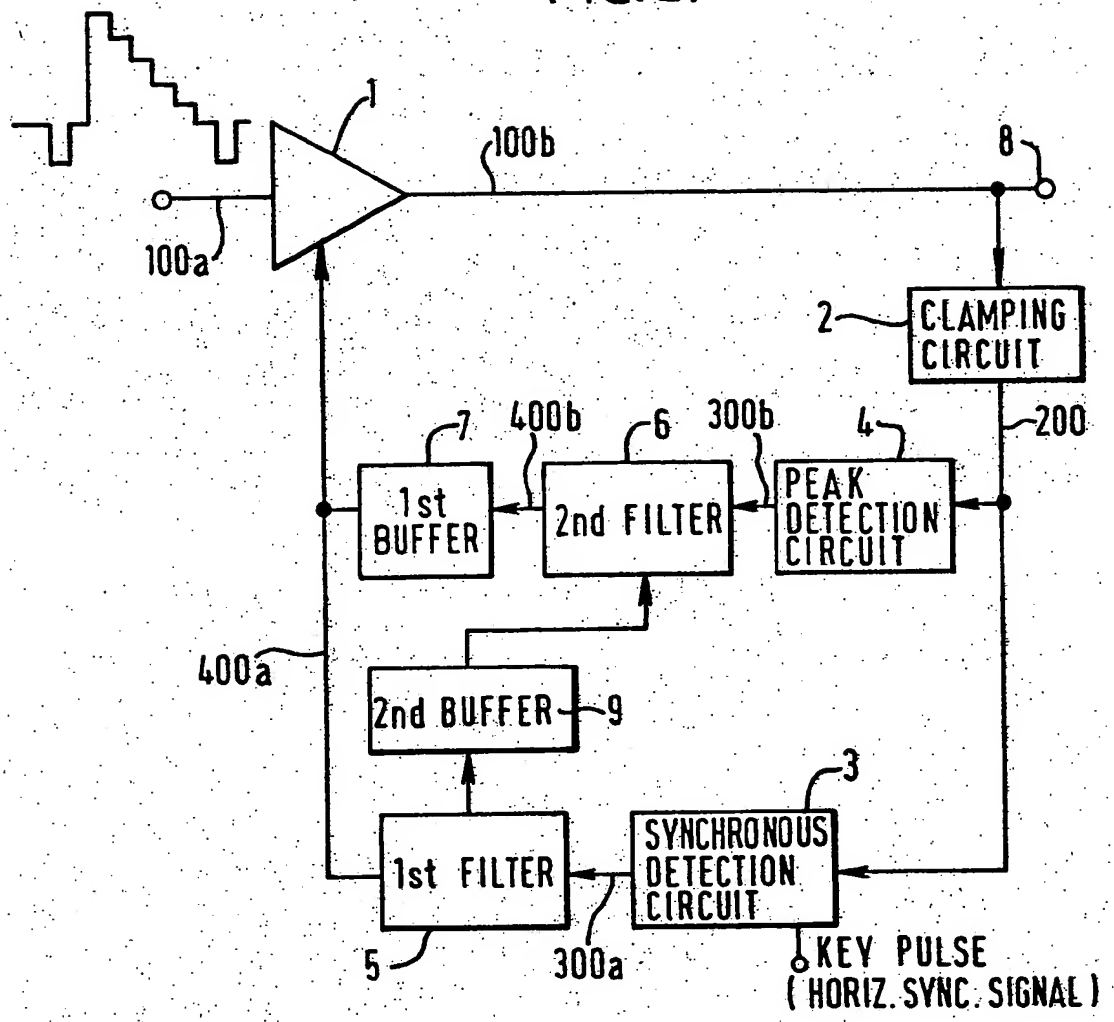
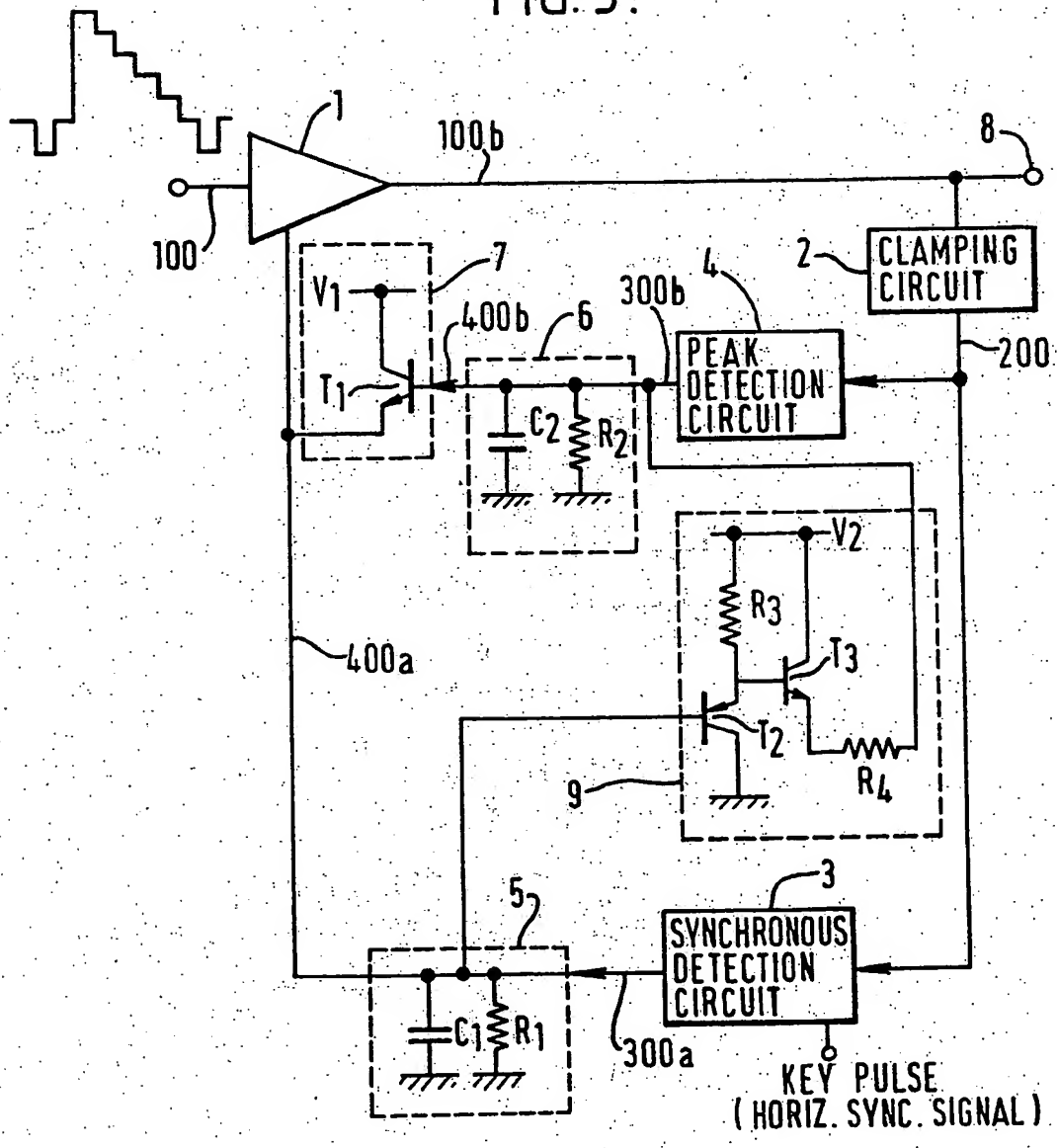

1
100b
8
100a
2
CLAMPING CIRCUIT
200
7
400b
6
300b
4
1st BUFFER
2nd FILTER
PEAK DETECTION CIRCUIT
400a
2nd BUFFER
9
3
1st FILTER
SYNCHRONOUS DETECTION CIRCUIT
5
300a
KEY PULSE
( HORIZ. SYNC. SIGNAL )

FIG. 3.


1
100b
8
100
7
V1
T1
400b
6
300b
4
2
CLAMPING CIRCUIT
PEAK DETECTION CIRCUIT
200
C2
R2
V2
R3
T3
T2
R4
400a
9
5
3
SYNCHRONOUS DETECTION CIRCUIT
C1
R1
300a
KEY PULSE
(HORIZ. SYNC. SIGNAL)

SPECIFICATION

**Automatic gain control circuit**

The present invention relates to an automatic gain control (AGC) circuit, and more particularly, to an AGC circuit suitable for a television receiver, a video tape recorder or a video disc player.

Figure 1 is a block diagram showing an example of a known AGC circuit (Encyclopedia of Electrical & Electronics Engineering by Denkishein, Vol 25, pages 318-319). An input picture signal 100a is amplified by an amplifier 1 to a produce an output picture signal 100b with AGC as described in detail later. Output picture signal 100b is fed both to an output terminal 8, and to a clamping circuit 2. In clamping circuit 2, a tip-end level of a synchronous signal component of the output picture signal 100b is clamped to a predetermined fixed voltage to produce a tip-end clamped picture signal 200. Clamped picture signal 200 from clamping circuit 2 is applied to a synchronous detection circuit 3 and also to a peak detection circuit 4. The synchronous detection circuit 3 detects the pedestal or black level of the clamped picture signal 200 by a synchronous or keyed detection with reference to the tip-end level of the synchronous signal component under synchronization of a key pulse, for example, as shown, a horizontal synchronizing signal obtained from a flyback transformer (not shown). The peak detection circuit 4 detects a peak level of the picture signal by a peak detection with reference to the tip-end level of the synchronous signal component. A first level signal 300a detected by the synchronous detection circuit 3 is smoothed by a first filter 5 to produce a first AGC signal 400a. This first AGC signal 400a is applied to a control terminal of the amplifier 1 for controlling the gain of amplifier 1. As a result, an output picture signal 100b with synchronous detection AGC is obtained at output terminal 8 as mentioned above. In the synchronous detection AGC, an amplitude of the synchronous signal component in the picture signal 100a is controlled so as to be kept substantially constant.

Additionally a second level signal 300b detected by the peak detection circuit 4 is smoothed by a second filter 6 to produce a second AGC signal 400b. This second AGC signal 400b is also applied to the control terminal of amplifier 1 through a buffer 7 for controlling the gain of amplifier 1. As a result, the output picture signal 100b is obtained with peak detection AGC on output terminal 8, also as mentioned above. In the peak detection AGC, an amplitude of the picture signal 100a is controlled so as not to exceed a predetermined amplitude.

In the AGC circuits, the synchronous detection circuit 3 makes a synchronous detection AGC loop together with amplifier 1, clamping circuit 2, and first filter 5, whilst peak detection circuit 4 makes a peak detection AGC loop together with amplifier 1, clamping circuit 2, second filter 6 and buffer 7.

In the example of the known AGC circuits described above, the synchronous detection AGC loop operates so as to hold an amplitude of the first level signal 300a at a given level so that the synchronous signal component of the output picture signal 100b is held with its amplitude substantially constant. However, it may happen that the amplitude level of the output picture signal 100b exceeds the desired maximum level relatively. To overcome this, the peak detection AGC loop operates so as to limit the amplitude level of the output picture signal 100b to the maximum amplitude level. Accordingly, the amplitude level of the output picture signal 100b on output terminal 8 is so controlled that its picture signal amplitude is limited to within the maximum level, as well as the amplitude of its synchronous signal component being held constant.

When incorporating the known AGC circuit described above in a video tape recorder, the AGC circuit operates for preventing an overmodulation in the video tape recorder. For preventing overmodulation, the AGC circuit is required to have a rapid response. However, in the known circuit, as shown in Figure 1, the AGC circuit fails promptly to prevent the overmodulation, Because the second filter 6 has been discharged to the 0 volt state during the time when the peak detection AGC loop is deactivated, the peak detection AGC loop fails to bring amplifier 1 into the peak detection AGC state immediately after the peak detection AGC loop has been activated or started. This defect of a slow response is extremely inconvenient for the preventing of the overmodulation described above.

The present invention seeks to provide an AGC circuit having a more prompt loop response characteristic than the known AGC circuit.

Further the present invention seeks to provide an AGC circuit which is improved over the known circuit for preventing overmodulation in a video tape recorder incorporating the AGC circuit.

According to the present invention there is provided an automatic gain control (AGC) circuit for performing and AGC for a picture signal, said AGC circuit comprising:

an amplifier having an input terminal, an output terminal and a control terminal, said amplifier amplifying said picture signal applied to said input terminal under control of an AGC signal applied to said control terminal;

a clamping circuit connected to said output terminal of said amplifier for fixing a tip-end level of a synchronous signal component of said picture signal to a given level;

a synchronous detection AGC loop constituted by said amplifier, said clamping circuit, a synchronous detection circuit and a first filter, said synchronous detection circuit being connected to said clamping circuit for detecting a pedestal level of said picture signal by a synchronous detection with the reference to said tip-end level of said synchronous signal component, said first filter being connected between said synchronous detection circuit and said control terminal of said amplifier for smoothing said synchronous detection signal from said synchronous detec-

tion circuit and applying said smoothed synchronous detection signal as said AGC signal to said control terminal of said amplifier; and

a peak detection AGC loop constituted by said amplifier, said clamping circuit, a peak detection circuit and a second filter, said peak detection circuit being connected to said clamping circuit for detecting a peak level of said picture signal by a peak detection with reference to said tip-end level of said synchronous signal component, said second filter being connected between said peak detection circuit and said control terminal of said amplifier for smoothing said peak detection signal from said peak detection circuit and applying said smoothed peak detection signal as said AGC signal to said control terminal of said amplifier;

and said AGC circuit further comprising means connected between said first filter and said second filter for precharghing said second filter by a voltage following a voltage charge on said first filter when said synchronous detection AGC loop is activated but said peak detection AGC loop is deactivated.

For a better understanding of the present invention, reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 is a block diagram showing an example of a known AGC circuit;

Figure 2 is a block diagram showing an embodiment of an AGC circuit according to the present invention; and

Figure 3 is a circuit diagram showing in more detail the circuit of Figure 2.

An embodiment of the present invention will now be described in detail with reference to Figures 2 and 3 of the accompanying drawings. Throughout the drawings, like reference numerals and letters are used to designate like or equivalent elements for the sake of simplicity or explanation.

Referring now to Figure 2, there is shown an example of an AGC circuit according to the present invention. In the circuit of Figure 2, an input picture signal 100a is amplified by an amplifier 1 and produces an output picture signal 100b with AGC as described in detail later. Output picture signal 100b is fed both to an output terminal 8, and to a clamping circuit 2. In clamping circuit 2, the level of a synchronous signal contained in output picture signal 100b is clamped to a predetermined fixed voltage to produce a clamped picture signal 200. Clamped picture signal 200 from clamping circuit 2 is applied to a synchronous detection circuit 3 and also to a peak detection circuit 4. Synchronous detection circuit 3 detects the synchronous signal from tip-end clamped picture signal 200 by a synchronous or keyed detection in which the pedestal level of picture signal 100b is compared with a reference level under the control of some synchronous signal; as shown, the horizontal synchronising signal from a flyback transformer (not shown). The synchronous detection circuit 3 forms a synchronous detection AGC loop together with the clamping circuit 2, a first filter 5 and the amplifier 1.

As mentioned, in the synchronous detection AGC loop, the synchronous detection circuit 3 detects the synchronous signal from the clamped picture signal 200 by a synchronous or keyed detection. A first level signal 300a thus detected by the synchronous detection circuit 3, is smoothed by the first filter 5 to produce a first AGC signal 400a. First AGC signal 400a is applied to a control terminal of the amplifier 1 for controlling the gain of the amplifier. As a result, an output picture signal 100b with synchronous detection AGC is obtained on output terminal 8. In the synchronous detection AGC, an amplitude of the synchronous signal component in the picture signal 100a is controlled so as to be kept substantially constant.

Peak detection circuit 4 forms a peak AGC loop together with clamping circuit 2, a second filter 6, a first buffer 7 and amplifier 1. In the peak AGC loop, peak detection circuit 4 detects the peak or maximum level signal from clamped picture signal 200 by a peak detection. A second level signal 300b thus detected by peak detection circuit 4 is smoothed by the second filter 6 to produce a second AGC signal 400b. This second AGC signal 400b is also applied to the control terminal of amplifier 1 through a first buffer 7 for controlling the gain of amplifier 1. As a result, the output picture signal 100b is obtained with peak detection AGC on output terminal 8. In the peak detection AGC, an amplitude of the picture signal 100a is controlled so as not to exceed a predetermined amplitude.

Further, the first filter 5 is coupled to the second filter 6 through a second buffer 9. As a result a voltage charge in the first filter 5 is applied to the second filter 6 through this second buffer 9.

Referring now to Figure 3, the AGC circuit, in particular, the circuit connection between the second buffer 9 and its related circuits and their operations will be described in detail. In Figure 3, practical circuit arrangements for the first filter 5, the second filter 6, the first buffer 7 and the second buffer 9 are given. First filter 5 is, as shown, constituted by a parallel circuit of a capacitor C1 and a resistor R1, each having one end connected to the synchronous detection circuit 3 and the other end earthed. The first connection node of the first filter 5 and the synchronous detection circuit 3 is coupled to the control terminal of amplifier 1. The second filter 6 is constituted by a parallel circuit of a capacitor C2 and a resistor R2, each having one end connected to the peak detection circuit 4 and the other end earthed. The second connection node of the second filter 6 and the peak detection circuit 4 is coupled to the control terminal of amplifier 1 through a first buffer 7. First buffer 7 is constituted by a transistor T1, of which the base is connected to the second connection node, the emitter is connected to the first connection node, and the collector is connected to a power source line with source voltage V1. The second buffer 9 is formed by transistors T2 and T3. The base of transistors T2 is connected to the first connection node, its emitter to a power source line with a source voltage V2 through a resistor R3, and its collector to the ground potential. The base of transistor T3 is connected to the emitter of transistor T2, its emitter to the second connection node through a resistor R4, and its collector to the power source line with source voltage V2.

The operation of the embodiment will be described below. When the synchronous detection circuit 3 is

keyed or activated, capacitor C1 in the first filter 5 is charged to the output potential of the synchronous detection circuit 3. The emitter potential of transistor T21 in the first buffer 7 rises with the charge voltage on capacitor C1 so as to bias transistor T1 to cut off. Therefore, whilst the synchronous detection AGC loop is activated, the peak detection AGC loop is deactivated. For this reason, the synchronous detection AGC loop performs its AGC operation described above without being affected by the peak detection AGC loop. Further, at this time, transistor T2 in the second buffer 9 is then biased at its base potential to the charge voltage of capacitor C1. Therefore, a current corresponding to the base bias, i.e. to the charge voltage flows through transistor T2. As a result, a current also flows through transistor T3. The current flowing through transistor T3 flows into the second filter 6 through the resistor R4 and charges the capacitor C2 in the second filter 6. The voltage charge on capacitor C2 is determined by the voltage drop of resistor R4. The charge voltage on capacitor C2 follows the charge voltage on capacitor C1 in the first filter 5. As a result, whilst the synchronous detection circuit 3 is operated, the second filter 6 is charged to a voltage following the charge voltage on capacitor C1 in the first filter 5, i.e. the second filter 6 is precharged in spite of the peak detection AGC loop being deactivated.

As a result, the peak detection AGC loop is able to enter promptly into the peak detection AGC operation stage after the peak detection circuit 3 is activated. By this loop, the gain of the amplifier 1 is promptly controlled to keep the amplitude level of the picture signal within the predetermined level. The response time of the synchronous detection AGC loop, when the operation returns from the peak detection AGC loop to the synchronous AGC loop, is determined by the time constant of the first filter 5, similarly to the known circuit.

According to the present embodiment, the second filter 6 in the peak detection AGC loop is precharged by the voltage following the charge voltage on the first filter 5 in the synchronous AGC loop, and the response of the peak AGC loop can thereby be improved. When the AGC circuit according to the present embodiment is used for a VTR and a television receiver, the function of preventing overmodulation can thereby be improved.

As described above, the AGC circuit of the present invention having a peak detection AGC loop and a synchronous detection AGC loop, has the effect of improving the response in time of the peak detection AGC loop by precharging the filter in the peak detection AGC loop while the synchronous detection AGC loop is operated.

CLAIMS

1. An automatic gain control (AGC) circuit for performing an AGC for a picture signal, said AGC circuit comprising:

an amplifier having an input terminal, an output terminal and a control terminal, said amplifier amplifying said picture signal applied to said input terminal under control of an AGC signal applied to said control terminal;

a clamping circuit connected to said output terminal of said amplifier for fixing a tip-end level of a synchrounous signal component of said picture signal to a given level;

a synchronous detection AGC loop constituted by said amplifier, said clamping circuit, a synchronous detection circuit and a first filter, said synchronous detection circuit being connected to said clamping circuit for detecting a pedestal level of said picture signal by a synchronous detection with reference to said tip-end level of said synchronous signal component, said first filter being connected between said synchronous detection circuit and said control terminal of said amplifier for smoothing said synchronous detection signal from said synchronous detection circuit and applying said smoothed synchronous detection signal as said AGC signal to said control terminal of said amplifier; and

a peak detection AGC loop constituted by said amplifier, said clamping circuit, a peak detection circuit and a second filter, said peak detection circuit being connected to said clamping circuit for detecting a peak level of said picture signal by a peak detection with reference to said tip-end level of said synchronous signal component, said second filter being connected between said peak detection circuit and said control terminal of said amplifier for smoothing said peak detection signal from said peak detection circuit and applying said smoothed peak detection signal as said AGC signal to said control terminal of said amplifier;

and said AGC circuit further comprising means connected between said first filter and said second filter for precharging said second filter by a voltage following a voltage charge on said first filter when said synchronous detection AGC loop is activated but said peak detection AGC loop is deactivated.

2. An automatic gain control (AGC) circuit according to claim 1, wherein said precharging means is a buffer means.

3. An automatic gain control (AGC) circuit according to claim 2, wherein said buffer means is formed by a first and a second transistor, the base of said first transistor being connected to said first filter and the base of said second transistor being connected to the emitter of said first transistor and its emitter to said second filter.

4. An automatic gain control (AGC) circuit according to claim 1 further comprising a buffer means connected between said synchronous detection AGC loop and said peak detection AGC loop for deactivating said peak detection AGC loop when said synchronous detection AGC loop is activated.

5. An automatic gain control (AGC) circuit according to claim 4, wherein said buffer means comprises a transistor, the base of which is connected to said second filter in said peak detection AGC loop whilst its emitter is connected to said first filter in said synchronous detection AGC loop.

6. An automatic gain control (AGC) circuit according to claim 1; further comprising a first buffer means connected between said synchronous detection AGC loop and said peak detection AGC loop for deactivating said peak detection AGC loop when said synchronous detection AGC loop is activated and wherein said precharging means comprises a second buffer means.

7. An automatic gain control (AGC) circuit according to claim 6, wherein said first buffer means comprises a first transistor, the base of which is connected to said second filter in said peak detection AGC loop whilst the emitter is connected to said first filter in said synchronous detection AGC loop and said second buffer means comprises second and third transistors, the base of said second transistor being connected to said first filter, the base of said third transistor being connected to the emitter of said second transistor and the emitter of said third transistor being connected to said second filter.

8. An automatic gain control (AGC) circuit substantially as hereinbefore described with reference to Figures 2 and 3 of the accompanying drawings.

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